attached to a facet of the chamber. (Support for the amendments can be found on page 21 lines 31-32 of Applicant's Specification) Critical dimensions, for example, are dimensional measurements accorded to features on a pattern-etched semiconductor wafer. Direct attachment of such a metrology tool to the chamber is advantageous in that the metrology tool can be used immediately after a wafer processing step that occurs in a similarly attached wafer processing tool.

In contrast, Sato et al. (U.S. Patent No. 5,766,360) does not disclose such a metrology tool that is directly attached to a facet of a wafer handling chamber. Specifically, Sato et al. ('360) merely describes inspection systems that are for performing measurements just on the thin films grown during semiconductor wafer fabrication. (See Column 1 Lines 47-53, Column 3 Lines 18-20 and Column 4 Lines 32-36) These inspection systems are not for measuring "critical dimensions". In other words, Sato et al. ('360) does not disclose a metrology tool for measuring dimensions of features on a pattern-etched semiconductor wafer. Although Sato et al. ('360) discloses a pre-processing that includes "dry-etching a natural oxide film on the surface of the wafer" (See Column 3 Lines 57-67), it does not disclose wafers that are pattern-etched. In fact, the dry-etched wafers disclosed in Sato et al. ('360) are different from pattern-etched wafers. For example, the dry-etched wafers in Sato et al ('360) comprised of "dry-etching a natural oxide film on the surface of the substrate" (See Column 3 Lines 62-63 and Column 7 Lines 46-47). That is, the dry-etching process involves etching evenly across the wafer without creating definitive patterns during the "layering process" of wafer fabrication. On the other hand, pattern-etched wafers are the result of etching unevenly to create definitive patterns across the wafer during the "patterning process" of wafer fabrication.

Accordingly, it is respectfully submitted that Sato et al. ('360) neither teach nor suggest the inventions of claims 59 and 65 as described above. Therefore, it is respectfully submitted that independent claims 59 and 65 are patentably distinct from the cited reference of Sato et al. ('360).

The Examiner's rejections of the dependent claims are respectfully traversed. However, to expedite prosecution, all of these claims will not be argued separately. Claims 60-64, and 66 each depend either directly or indirectly from independent claims 59 or 65 and, therefore, are respectfully submitted to be patentable over cited art for at least the reasons set forth above with respect to claims 59 or 65. Further, the dependent claims require additional elements that when considered in context of the claimed inventions further patentably distinguish the invention from the cited art.

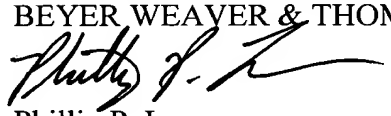
Applicant has added new claims 67-74. Support for all the new claims can be found throughout the specification. For example, among other places, support for claims 67 and 68 is found on p. 21 lines 31-32. Support for claims 69 and 70 is found on p. 21 lines 2-8. Similarly, support for claims 71-74 is found on p. 21 lines 15-32.

SUMMARY

It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 500388 (Order No. KLA1P001C1). A duplicate copy of the transmittal sheet for this amendment is enclosed for this purpose.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

59. (Amended Once) A semiconductor manufacturing system comprising:

a wafer handling chamber having a plurality of facets, the wafer handling chamber containing a vacuum environment;

a plurality of wafer processing tools, each of the tools being attached to a respective facet on the wafer handling chamber;

a **first** metrology tool attached to one of the facets of the wafer handling chamber, wherein the **first** metrology tool measures **[physical parameters] critical dimensions** on **pattern-etched** semiconductor wafers; and

a wafer handler located within the wafer handling chamber for transporting **semiconductor** wafers between each of the plurality of facets.

61. (Amended Once) A semiconductor manufacturing system as recited in claim 60 wherein the **[optical]** inspection tool is a modular optical inspection system that **[includes] comprises:**

a plurality of modular inspection subsystems each configured to detect defects on a portion of a semiconductor wafer;

a mechanism for moving at least one of the semiconductor wafer and the plurality of modular inspection subsystems with respect to one another; and

a master processor configured to process data delivered from at least some of the modular inspection subsystems, wherein a first one of the plurality of modular inspection subsystems includes a local processor configured to process data collected by the first modular inspection subsystem.

62. (Amended Once) A semiconductor manufacturing system as recited in claim 59 **[wherein] further comprising:**

a second metrology tool, wherein the **second** metrology tool is an ellipsometer configured to measure the thickness of a layer on the surface of the semiconductor wafer.

63. (Amended Once) A semiconductor manufacturing system as recited in claim 59 wherein at least one of the process**ing** tools is a type of tool selected from the group consisting of a CVD reactor, an etcher, and a stripper.

65. (Amended Once) A method of manufacturing a semiconductor wafer comprising:

providing a wafer handling chamber having a plurality of facets, the wafer handling chamber containing a vacuum environment;

providing a plurality of wafer processing tools, each of the tools being attached to a respective facet on the wafer handling chamber;

providing a metrology tool attached to one of the facets of the wafer handling chamber, wherein the metrology tool measures **[physical parameters]** **critical dimensions** on **pattern-etched** semiconductor wafers;

transferring the semiconductor wafer from one of the plurality of wafer processing tools to the metrology tool; **and**

measuring the dimension of at least one feature on the semiconductor wafer with the metrology tool.

APPENDIX: CURRENTLY PENDING CLAIMS

59. (Amended Once) A semiconductor manufacturing system comprising:

a wafer handling chamber having a plurality of facets, the wafer handling chamber containing a vacuum environment;

a plurality of wafer processing tools, each of the tools being attached to a respective facet on the wafer handling chamber;

a first metrology tool attached to one of the facets of the wafer handling chamber, wherein the first metrology tool measures critical dimensions on pattern-etched semiconductor wafers; and

a wafer handler located within the wafer handling chamber for transporting semiconductor wafers between each of the plurality of facets.

60. A semiconductor manufacturing system as recited in claim 59 further comprising:

an inspection tool attached to one of the facets of the wafer handling chamber, wherein the inspection tool reviews semiconductor wafers for defects.

61. (Amended Once) A semiconductor manufacturing system as recited in claim 60 wherein the inspection tool is a modular optical inspection system that comprises:

a plurality of modular inspection subsystems each configured to detect defects on a portion of a semiconductor wafer;

a mechanism for moving at least one of the semiconductor wafer and the plurality of modular inspection subsystems with respect to one another; and

a master processor configured to process data delivered from at least some of the modular inspection subsystems, wherein a first one of the plurality of modular inspection subsystems includes a local processor configured to process data collected by the first modular inspection subsystem.

62. (Amended Once) A semiconductor manufacturing system as recited in claim 59 further comprising:

a second metrology tool, wherein the second metrology tool is an ellipsometer configured to measure the thickness of a layer on the surface of the semiconductor wafer.

63. (Amended Once) A semiconductor manufacturing system as recited in claim 59 wherein at least one of the processing tools is a type of tool selected from the group consisting of a CVD reactor, an etcher, and a stripper.

64. A semiconductor manufacturing system as recited in claim 59 further comprising:

a wafer storage cassette that is attached to one of the facets on the wafer handling chamber.

65. (Amended Once) A method of manufacturing a semiconductor wafer comprising:

providing a wafer handling chamber having a plurality of facets, the wafer handling chamber containing a vacuum environment;

providing a plurality of wafer processing tools, each of the tools being attached to a respective facet on the wafer handling chamber;

providing a metrology tool attached to one of the facets of the wafer handling chamber, wherein the metrology tool measures critical dimensions on pattern-etched semiconductor wafers;

transferring the semiconductor wafer from one of the plurality of wafer processing tools to the metrology tool; and

measuring the dimension of at least one feature on the semiconductor wafer with the metrology tool.

66. A method of manufacturing a semiconductor wafer as recited in claim 65 further comprising:

providing an inspection tool attached to one of the facets of the wafer handling chamber, wherein the inspection tool reviews semiconductor wafers for defects;

transferring the semiconductor wafer from the metrology tool or one of the wafer processing tools to the inspection tool; and

inspecting the semiconductor wafer for defects using the inspection tool.

67. (Added Claim) A method of manufacturing a semiconductor wafer as recited in claim 65 wherein the metrology tool is an optical detector.

68. (Added Claim) A semiconductor manufacturing system as recited in claim 59 wherein the first metrology tool is an optical detector.

69. (Added Claim) A semiconductor manufacturing system comprising:

a wafer handling chamber having a plurality of facets, the wafer handling chamber containing a vacuum environment;

a plurality of wafer processing tools, each of the wafer processing tools being attached to a respective facet on the wafer handling chamber;

at least two inspection tools, wherein each inspection tool is configured to generate a defect report for an associated wafer processing tool; and

a computer containing a defect database that collects defect reports from each of the inspection tools, whereby statistical process control of each associated wafer processing tool is performed.

70. (Added Claim) A semiconductor manufacturing system as recited in claim 69 wherein there is an inspection tool associated with each of the wafer processing tools.

71. (Added Claim) A semiconductor manufacturing system, comprising:

a wafer handling chamber having a plurality of facets, the wafer handling chamber containing a vacuum environment;

a plurality of wafer processing tools, each of the wafer processing tools being attached to a respective facet on the wafer handling chamber; and

a modular inspection tool attached to one of the facets of the wafer handling chamber, the modular inspection tool including a plurality of inspection sensors and metrology sensors, whereby the metrology sensors measure critical dimensions on pattern-etched semiconductor wafers.

72. (Added Claim) A semiconductor manufacturing system as recited in 71 wherein the inspection sensors and metrology sensors are interleaved.

73. (Added Claim) A method of inspecting semiconductor wafers on a wafer handling chamber, comprising:

providing a wafer handling chamber having a plurality of facets, the wafer handling chamber containing a vacuum environment;

providing a plurality of wafer processing tools, each of the wafer processing tools being attached to a respective facet on the wafer handling chamber;

providing a modular inspection tool for attaching to a facet of the wafer handling chamber wherein the modular inspection tool includes a plurality of interleaved inspection and metrology sensors;

performing a first scan of a semiconductor wafer with the modular inspection tool wherein the inspection sensors are used to inspect the wafer for defects; and

performing a second scan of the semiconductor wafer with the modular inspection tool wherein the metrology sensors are used to measure critical dimensions on the wafer.

74. (Added Claim) A method of inspecting semiconductor wafers on a wafer handling chamber as recited in claim 73, further comprising:

transferring the semiconductor wafer from one of the plurality of wafer processing tools to the modular inspection tool.